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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,606	03/01/2004	Jiong-Ping Lu	TI 37479	9593
23494	7590	07/20/2006	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED			TRAN, LONG K	
P O BOX 655474, M/S 3999			ART UNIT	
DALLAS, TX 75265			PAPER NUMBER	

2818

DATE MAILED: 07/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/790,606

Applicant(s)

LU, JIONG-PING

Examiner

Long K. Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 July 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10, 12, 14, 15 and 17-22 is/are pending in the application.
- 4a) Of the above claim(s) 1-9, 17 and 20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 10, 12, 14, 15, 18, 19, 21 and 22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

1. The allowable subject matter of claims 13 – 15 in the Non Final Office Action, on 11/28/05, and the Final Office Action, on 05/03/2006, are withdrawn by the Examiner.
2. This office action is in response to Amendment filed on 07/10/2006.
3. Claims **11, 13** and **16** have been cancelled.
4. Claims **1 – 9, 17** and **20** have been withdrawn
5. Claims **10** and **14** have been amended.
6. Claims **10, 12, 14, 15, 18, 19, 21** and **22** are presented for examination.

### ***Claim Objections***

7. Claim 10 is objected to because of the following informalities: at line 10, delete "blanket"; typo error. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims **10, 14, 15, 19, 21** and **22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Amos et al. (US Patent No. 6,846,734) in view of Lochtefeld (US. Patent Application Publication no. 2006/0024869).
10. Regarding claim **10**, Amos, figures 1 – 16, discloses a method for manufacturing a semiconductor device, comprising:  
  
placing a layer of gate oxide material (18) over a substrate (10); and

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forming a silicided gate electrode 38, (62), (64) over said gate oxide material (18) including:

forming a layer of doped polysilicon material (20) over said layer of gate oxide material (18);

forming a layer of a metal alloy ((38), (58); column 6, lines 41 – 67; column 7, lines 1 – 25; and column 9, lines 10 – 40) comprising a first metal, and a second metal over said layer of polysilicon material (20);

Annealing said layer of an alloy (58) comprising a first metal and said second metal to form a layer of silicided gate electrode material ((62) / (64), column 9, line 41 to column 10, line 34).

Amos fails to teach step of implanting a dopant into the layer of polysilicon material affecting a work function of the silicided gate electrode

However, Lochtefeld discloses method of making a device (CMOS; [0004]) similar to that of Amos that includes step of implanting a dopant into a polysilicon gate material (520, figure 5; [0056]) – [0058] of a silicided gate electrode to achieve a desired conductivity ([0003] and [0071]).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include implanting a dopant into a blanket polysilicon gate material of Amos as taught by Lochtefeld in order achieve a desired conductivity which appears to affect a work function of the silicided gate electrode as the claimed invention.

Regarding claims 14 and 15, Amos discloses a capping layer (60), comprising a transition metal nitride such as TiN, is formed on the surface of the metal alloy (58)

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(column 9, lines 42+) for preventing oxygen from diffusing into the structures which in turn effect a doping profile of the dopant.

Regarding claim **19**, Amos discloses forming source/drain regions (28; figures 4 – 16) in the substrate 14 and forming silicided source/drain contact (52, figures 12 – 16) regions in the source/drain regions 28 subsequent to forming the silicided gate electrode (62, figures 14 – 16). See column 8, line 35 to column 10, line 50.

Regarding claims **21** and **22**, Amos discloses the first metal for the alloy layer are Co or Ni and the second metal are Co or Ni (column 9, lines 10 – 25).

11. Claim **12** is rejected under 35 U.S.C. 103(a) as being unpatentable over Amos et al. (US Patent No. 6,846,734) in view of Lochtefeld (US. Patent Application Publication no. 2006/0024869) and further in view of Thakur (US. Patent no. 6,028,002).

12. Regarding claim **12**, Amos and Lochtefeld disclose the claimed invention of claim 10 except for patterning said blanket layer of silicided gate electrode material to form a silicided gate electrode.

However, Thakur shows a silicided stacked gate electrode comprising layers 22, 23, 24 (metal silicide), and 25 being patterned and etched to form metal silicided gate electrode (31, figure 3; column 3, lines 38 – 40).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide a step of patterning a blanket layer of silicided gate electrode material as shown by Thakur for patterning the blanket layer of silicided gate

electrode material of Amos and Lochtefeld, in order to complete the process of forming the transistor gate (column 4, lines 29 – 31).

**13.** Claim **18** is rejected under 35 U.S.C. 103(a) as being unpatentable over Amos et al. (US Patent No. 6,846,734) in view of Lochtefeld (US. Patent Application Publication no. 2006/0024869) and further in view of remarks

Regarding claim **18**, Amos discloses the claimed invention of claim 10 and also teaches the alloy layer comprising a first metal (Co or Ni) and at least another metal (Co or Ni; different from the first metal) having a ratio range of 0.1 to 50 atomic % (column 9, lines 10 – 29) but fails to disclose the ratio of an atomic percent of said first metal to said second metal in said silicide gate electrode ranges from about 9:1 to about 2:3 as the instant claim. In other words, because the reference does not disclose exactly as claimed, it cannot be said that the reference anticipates the claim. However since the reference's ratio range overlaps the claimed ratio range of about 9:1 to about 2:3, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the reference's ratio range to achieve the claimed ratio range, since changing from one range to another range would be obvious to one of ordinary skill in the semiconductor technology art at the time the invention was made.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MinSun Harvey or Matthew Smith can be reached on 571-272-1835 or 571-272-1907 (Smith). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LKT

A handwritten signature in black ink, appearing to read "WARM", with a horizontal line drawn underneath it.

July 17, 2006